PulseGen
User’s Manual

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PulseGen generates 5 – 1000v, 1KHz to 10MHz, low duty cycle, high current pulse waveforms to drive low impedance loads. All aspects of the pulse waveform are programmable, frequency, voltage, delay, and the number of pulses. There are two methods for triggering the pulse waveform, internal and external. In external mode a TTL pulse trigger is input to the board and the pulse waveform is output after a programmable delay from the trigger. In internal mode an internal pulse trigger is generated with a programmable period and the pulse waveform is output on the falling edge of the pulse enable. A 100MHz master clock is used to provide 10ns resolution on all timing parameters. FIGURE 1 shows the PulseGen board and FIGURE 2 shows a 10MHz, 700v, waveform generated by the board.

The PulseGen board is mated to an MSP430 Launchpad™ board from Texas Instruments. The Launchpad™ provides two functions, USB interface and program control. PulseGen includes a graphical user interface which runs under Windows and the Launchpad™ board provides a USB interface between Windows and the PulseGen board. Realtime control signals on the PulseGen board are generated by a PLD and the Launchpad™ provides the programming interface to the PLD.

FIGURE 3 shows the LaunchPad™ board attached to the PulseGen board.
SPECIFICATIONS

Performance
Frequency: 1KHz to 10MHz, programmable
Voltage: 5v to 1000v, programmable
Number of Pulses: 1 to 31, programmable
Trigger Modes: Internal or External
Internal Trigger Mode Burst Interval: 200us to 100ms, programmable, 40us steps
Delay from External Trigger: 200ns to 1000us, programmable, 20ns steps
Pulse Rise Time, 0 - 1000v: 20ns
Pulse Fall Time, 0 - 1000v: 10ns
Load Current: 3.5a max

User Interface
Operates under Windows XP, 7, 8, and 10

Board
Operating Temperature 0°C to 50°C
Size 3.0” x 3.3”
Power Input +12v +/- 5%, 0.
External Trigger Input TTL levels
Internal Trigger Output TTL levels

Connectors
J1 SMA Pulse output
J2 Auxiliary functions, this connector is not installed
J3 header This connector attaches to a PLD
J4, J5 header These headers mate with the Launchpad™ board.
J6 SMB Internal pulse trigger output
J7 SMB External pulse trigger input
J8 Barrel Conn. Power jack, +12v input.
GRAPHICAL USER INTERFACE

All the programmable parameters available on the PulseGen board are available through the user interface shown in FIGURE 4. Voltage, Frequency, and Number of Pulses are programmable in both internal and external trigger modes. Delay is available in external trigger mode and Burst Interval is available in internal trigger mode. In external trigger mode the Delay parameter sets the delay of the pulse output from the rising edge of the external trigger. In internal mode the Burst Interval sets the period of the pulse waveform. The pulse waveform starts on the falling edge of the internal pulse trigger.

Other fields in the user interface include Pulser Enable and Connected. When the Windows computer hosting the user interface connects to the Launchpad™ board via a USB link the Connected field is displayed in green. If the user interface is executed and there is no USB link the user interface will continue to try and connect. The Pulser Enable field turns the pulser output on and off.

Parameters entered into the LaunchPad™ through the user interface are stored in non-volatile memory. Thus PulseGen maybe programmed, removed from the user interface, and then operate autonomously.

See the Quick Start guide for installation of the user interface.
**COMMAND LINE INTERFACE**

The PulseGen board can also be programmed via a terminal program through a command line interface. The commands are:

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pulse Frequency</td>
<td>#PF &lt;1 – 10,000&gt;</td>
<td>KHz</td>
</tr>
<tr>
<td>Pulse Amplitude</td>
<td>#PA &lt;5 – 1,000&gt;</td>
<td>Volts</td>
</tr>
<tr>
<td>Number Pulses</td>
<td>#NP &lt;1 – 31&gt;</td>
<td>Pulses</td>
</tr>
</tbody>
</table>
| Trigger Mode      | #TM <0 | 1>              | 0 – Internal Trigger  
|                   |                   | 1 – External Trigger |
| Pulser Enable     | #PE <0 | 1>              | 0 – Pulser Off  
|                   |                   | 1 – Pulser On      |
| External Mode Pulse Delay | #PD <5 – 50000> | 20ns counts |
| Internal Mode Burst Interval | #BI <5 – 4000> | 40us counts |
| Status Information| #SI               |                    |
| PF                | Pulser Frequency  |                    |
| PD                | Pulser Delay      |                    |
| NP                | Number Pulses     |                    |
| PE                | Pulser Enable     |                    |
| PA                | Pulser Amplitude  |                    |
| TM                | Trigger Mode      |                    |
| BI                | Burst Interval    |                    |
| FV                | Firmware Version  |                    |
CIRCUIT DESCRIPTION

The pulse generation circuit is shown in FIGURE 5. The output stage is a high side / low side circuit using discrete FETs with low gate charge and low gate / drain capacitance to provide the highest operating frequency. The high voltage power supply is only 1.5 watt but the capacitor shown in FIGURE 5 provides an instantaneous high current source to drive the low impedance loads required of this circuit. The capacitor is limited in the charge it can hold which limits the load current and the number of pulses which can be generated.

Timing control of the pulse waveform is performed by a PLD. The PLD uses a 100MHz clock to generate the timing parameters such as frequency and delay with 10ns resolution. Of great importance to the quality of the pulse waveform are the rise and fall times of the pulse. FIGURES 6 and 7 show the PulseGen output waveforms at 10MHz with a voltage of 700v and 70v. The same waveforms are shown in FIGURES 8 with a 100KHz frequency.
Delay is a parameter that is used in external trigger mode to delay the pulse output from an external trigger input. The minimum and maximum delays are shown in FIGURES 9a and 9b. In FIGURE 9a a 10MHz pulse is shown delayed from the external trigger by 200ns and in FIGURE 9b a 10KHz pulse is delayed by 1ms. The 200ns minimum delay is caused by a digital filter used to prevent a sloppy external trigger from causing problems.